Advance Training Plan for DSP using Xilinx System Generator

Course Overview:

This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost Digital Signal Processing designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools and hardware co-simulation verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification by using Xilinx FPGA capabilities.

Who Should Attend?

System engineers, system designers, logic designers and experienced hardware engineers interested in DSP design training who are implementing DSP algorithms using the MathWorks MATLAB® and Simulink® software and want to use Xilinx System Generator for DSP design.

Prerequisites

- Basic understanding of signal processing theory.
- Advantage if experience with the MATLAB and Simulink software.

Course Objectives:

- Describe the System Generator design flow for implementing DSP functions.
- Identify Xilinx FPGA capabilities and implement a design from algorithm concept to hardware simulation.
- List various low-level and high-level functional blocks available in System Generator.
- Run hardware co-simulation.
- Identify the high-level blocks available for FIR and FFT designs.
- Implement multi-rate systems in System Generator.
- Integrate System Generator models into the Vivado IDE.
- Design a processor-controllable interface using System Generator for DSP.
- Generate IPs from C-based design sources for use in the System Generator environment

Course Outline:

Module 1: Introduction

- FPGAs for DSP
- Introduction to System Generator

- Simulink Basics.Digital Systems

Module 2: Arithmetic Operations

- Fixed Point Format-Signed and Unsigned (with or without binary point)
- Gateway In & Out
- Saturation and Wrap in fixed-point numbers
- Applications of Round and Truncate in fixed point while arithmetic operations
- Hardware Cost of Saturation, Wrap, Round and Truncation
- Addition, Subtraction, Multiplication, Division, Scaling and Shifting
- Complex arithmetic- Complex multiplication, conjugate etc.

Module 3: Library Overview

- Use of blocks available inside Xilinx Block sets' Library- Basic blocks
- Handshaking blocks- FIFO, BLOCK RAM etc
- Signal Processing Blocks- FFT, FIR etc
- Data storing blocks- ROM
- Black Box- HDL import

Module 4: CORDIC

- Arithmetic Functions in Circular Coordinates
- Implementations
- CORDIC Compiler

Module 5: FIR & IIR Filtering

- Sampling, Sub-Sampling, Nyquist-Criterion, Mixing, Quadrature Modulator &I-Q
- Single Rate and Multirate Filters
- MAC filters
- Interpolation and Decimation
- Difference between Upsampling, Interpolation, Downsampling and Decimation.
- Half-Band Filters and their implementation
- Interpolation FIR filter and its implementation using FDA Tool
- Decimation FIR Filter- with various windowing techniques and its implementation using FDA Tool
- Poly-Phase Filters
- IIR Filter and its implementation using FDA Tool
- Effects of Quantization and the importance of ENOB

Module 6: XILINX DSP48x BASED FIR FILTER IMPLEMENTATION

- Directly Targeting DSP 48x block
- Symmetric Filters
- Multi-Rate Filter with DSP48x Blocks and optimisation using Hardware Oversampling.

Module 7: LOW PASS CASCADED INTEGRATED COMB (CIC) FILTERS

- Brief Overview of Decimation and Interpolation
- CIC Filters Theory and its Construction
- Interpolation and Decimation with CIC
- CIC Compiler
- Compensation FIR Filter

Module 8: NUMERICALLY CONTROLLED OSCILLATOR (NCO)

- Look Up Table Technique
- DDS Compiler and Phase Truncation techniques
- Sine wave generation using DDS Compiler
- Applications

Module 9: Introduction to Analog Communication

- Analog modulation schemes
- Analog Transmitter- AM-SSB/AM-DSB/FM
- Analog Receiver- AM-SSB/AM-DSB/FM

Module 10: Introduction to Digital Communication

- Basic Modulation Schemes like PSK, FSK, QAM, OFDM etc.
- PSK-based Modulator
- OFDM Modulator
- Pulse Shaping and Matched Filtering and its implementation
- PSK-based Demodulator
- OFDM Demodulator
- Communication Link
- Channels and Channel Equalization
- Eb/No Vs BER plots for PSK schemes Compiler Directives

Module 11: Digital Up Conversion and Digital Down Conversion

- Digital Up Converter and Digital Down Converters

- Implementation Using either FIR filters or CIC filters
- SNR improvement in DDC. Hierarchical Names

Module 12: SYNCHRONIZATION

- Phase-Locked Loop (PLL)
- Timing Synchronization
- Carrier Synchronization- Phase and Frequency

Module 13: MULTIPLE CLOCK DOMAIN

- Use of CE, Asynchronous Reset
- Timing and Clocking
- Synchronization Mechanism
- Resource Estimation
- Auto-generated Clock Enable Logic

Module 14: AXI4-Lite Interface Synthesis

- Package a System Generator for DSP design with an AXI4-Lite interface and integrate this packaged IP into a Zynq® All Programmable SoC processor system

Module 15: CREATING BITSTREAM, USE OF CHIPSCOPE PRO/LOGIC ANALYZER AND H/W COSIM

- Analyze Design using Timing and Power Report
- Creating HDL
- Creating IP
- Creating Bitstream
- Analyze Complete Design using CHIPSCOPE/LOGIC ANALYZER
- Hardware Co-Simulations

Assessments:

- Quizzes and Assignments
- Lab Work and Practical Sessions
- Project Evaluations
- Final Examination
- Internship Performance and Report

Resources:

- Course Materials and Slides
- Arduino Kits and Sensors
- Online Tools and IDEs
- Access to IoT Cloud Platforms
- Community Forums and Support

Duration:

- 4 weeks with 2-3 hours of lectures per week and 4-5 hours of project work per week

Additional Features:

- Live Instructor Classes
- Doubt Sessions
- Project Hands-On
- Certification on Course Completion
- Recorded Sessions
- Evening Classes

For Registration/More Details: https://www.nationin.com/contact-us